**UNIT -1**

**2 MARKS**

1. Convert (126)10 to Octal number and binary number.
2. Convert (0.6875)10 to binary.
3. Convert (23.625)10 to octal.
4. Find the octal equivalent of the hexadecimal number DC.BA.
5. What are the different ways to represent a negative number?
6. What is meant by non weighted codes?
7. Write short notes on weighted binary codes.
8. What is meant by self-complementing codes?
9. Represent 3856 in BCD and 2421 code.
10. Convert the following Excess-3 numbers to decimal numbers (a)1011 (b)1001 0011 0111
11. Simplify the following Boolean equation F= x’y’+xy+x’y
12. Simplify the expression Z = AB+A(.
13. State the principle of duality.
14. State DeMorgan’s theorem.
15. State and prove consensus theorem.
16. Prove the following using Demorgan’ theorem [(X+Y)’+(X+Y)’]’= X+Y
17. Construct OR gate and AND gate using NAND gates.
18. Given the two binary numbers X = 1010100 and Y = 1000011, perform the subtraction Y – X by using 2’s complements.
19. Given two binary numbers A=1010010 and B=1000011, find A-B and B-A using 2’s complements.
20. What is the main difference between canonical and standard form?
21. Describe the importance of don’t care conditions.
22. What is a prime implicant?
23. What are the limitations of K-map.
24. Define minterm and maxterm.
25. What is meant by multilevel gates networks?
26. Discuss the NOR operation with a truth table.
27. Implement AND gate using only NOR gate .

**13 MARKS**

1. (i) Convert the following numbers to decimal (11011.101)2,(5432)6

(ii) Perform the following arithmetic operations using 2’s complement arithmetic.

(11011100)2-(10011011)2

(iii)Express the following functions in sum of minterms and product of maxterms

F(A,B,C,D)=A’B+BD+AC’

1. Express the function F=A+B’C (8)

i)Canonical SOP

ii)Canonical POS

1. Simplify the following in (1)SOP (2)POS:

(i)x’z’+y’z’+yz’+xy

(ii)AC’+B’D+A’CD+ABCD

(iii)(A’+B’+D’)(A+B’+C’)(A’+B+D’)(B+C’+D’)

1. Simplify the following expression:

Y(A,B,C,D)=m1+m3+m4+m7+m8+m9+m10+m11+m12+m14

1. Simplify using K-map

F(A,B,C,D)=∑m(7,8,9)+d(10,11,12,13,14,15) (8)

1. Simplify the Boolean function using K-map F(w,x,y,z)= ∑m(1,3,7,11,15) which has the don’t cares d(w,x,y,z)= ∑(0,2,5).
2. Reduce the following function using K-map.

F(A,B,C,D)=Πm(0,2,3,8,9,12,13,15)

1. Simplify the logical expression using K-map in SOP and POS form

F(A,B,C,D)=∑m(0,2,3,6,7)+d(8,10,11,15)

1. Determine the MSP form of the switching function

F(a,b,c,d)= ∑m(0,2,4,6,8)+d(10,11,12,13,14,15)

1. i)Simplify the given boolean function in POS form using Kmap and draw the logic diagram using Only NOR gates F(A,B,C,D)= ∑m (0,1,4,7,8,10,12,15)+d(2,6,11,14).

ii)Convert 78.510 into binary.

iii)Find the dual and complement of the following Boolean expression xyz’+x’yz+z(xy+w).

1. Simplify the Boolean function : F (A, B, C, D,E) = ∑m (0,1,3,7,13,14,21,26,28) + ∑d(2,5,9,11,17,24)
2. Implement the following function only with NAND gates using minimum number of gate inputs F(A,B,C,D)=AB+CD.
3. Simplify the following expressions and implement them with two-level NAND gate circuits:

(i)AB’+ABD+ABD’+A’C’D’+A’BC’

(ii)BD+BCD’+AB’C’D’

1. Simplify the following Boolean function using K-map and implement using NOR gates.

F(a,b,c,d)= ∑m(0,2,5,8,10,15)+d(4,14)

1. Implement a full adder using NOR gates only.

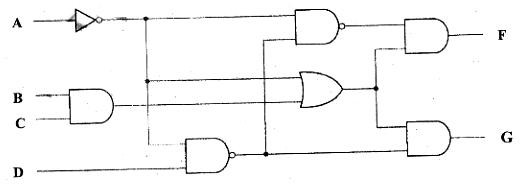
**UNIT -2**

**2 MARKS**

1. Define combinational circuits.
2. Mention the design procedure of combinational circuits.
3. Design a combinational circuit with 3 inputs and 1 output. The output is 1 when the binary value of the inputs is less than 3. The output is 0 otherwise.
4. What is magnitude comparator?
5. Implement a 4 bit even parity generator.
6. Implement a 4 bit even parity checker.
7. Write the data flow description of a 4-bit comparator.
8. What are binary decoders?
9. Write the truth table of 2 to 4 line decoder and draw its logic diagram.
10. What is priority encoder?
11. Draw the truth table and circuit diagram of 4 to 2 encoder.
12. What is multiplexer? Show the block diagram of 4 x 1 mux.
13. Draw the circuit of 2:1 mux.
14. Define multiplexer.
15. Draw the truth table of 2:1 MUX.
16. Implement a full adder with 4×1 multiplexer.
17. Implement the following Boolean function using 8:1 multiplexer F(A,B,C)= ∑m(1,3,5,6)
18. Draw 1:8 Demux using two 1:4 Demux
19. Distinguish between a decoder and a demultiplexer.
20. Design a 2-bit binary to gray code converter.
21. Draw the 4 bit Gray to Binary code converter.
22. Draw the 4 bit Binary to Gray code converter.

**13 MARKS**

1. Design a full adder using half adders.
2. Design a full subtractor using half subtractors. (8)
3. Implement a binary multiplier using logic circuits.
4. Design a 4-bit binary adder-subtractor circuit.
5. Design a combinational circuit that accepts a 3-bit binary number and generates a 6-bit binary number output equal to the square of the input number. Write the high level behavior VHDL description of the circuit.
6. Explain carry look ahead adder with logic diagram.
7. Construct a BCD adder circuit and write a HDL program module for the same.
8. Design BCD to Excess-3 converter. (8)
9. Design a logic circuit that accepts a 4-bit Gray code and converts it into a 4-bit binary code.
10. Explain the Analysis procedure. Analyze the following logic diagram.



1. Design a 5 to 32 decoder using combination of 2 to 4 and 3 to 8 decoders.
2. Implement the Boolean function using 8:1 Mux

F(A,B,C,D)=∑m(0,1,3,4,8,9,15)

1. Implement the following Boolean function with an 8-to-1 line multiplexer and an inverter F(A,B,C,D)= ∑m(2,4,6,9,10,11,15).
2. Implement the following Boolean function with an 8-to-1 line multiplexer

F(W,X,Y,Z)=W’XZ’+WYZ+X’YZ+W’Y’Z

1. Design 32 to 1 mux using four 8 to 1 mux and 2 to 4 decoder.
2. Design a 4-bit magnitude comparator with three outputs
3. Construct a 4 to 16 line decoder with an enable input using five 2 to 4 line decoders with enable inputs.
4. Design a BCD to 7 segment decoder and implement it by using basic gates.
5. Discuss the need and working principle of Carry Look ahead adder.
6. Construct a 4-bit priority encoder.
7. State the different modelling techniques used in HDL.
8. Write HDL for 4-bit adder.
9. Write a VHDL code to realize a full adder using
10. Behavioral model
11. Structural model

**UNIT-3**

1. **MARKS**
2. What is meant by edge triggered flip flops?
3. Draw the logic diagram and write the function table of D latch.
4. Differentiate latch and flip flop.
5. What is the drawback of SR flipflop?
6. Draw truth table of JK flip flop.
7. State the operation of T flip-flop.
8. Give the block diagram of master-slave D flip- flop.
9. What is ring counter?
10. How many states are there in 3-bit ring counter? What are they?
11. With reference to a JK flip-flop, what is racing?
12. What is synchronous sequential circuit?
13. Differentiate sequential and combinational circuit.
14. Differentiate between synchronous and asynchronous sequential circuit.
15. Convert T flip flop to D flip flop.
16. How many flip flops are required to design a mod 25 counter?
17. How synchronous counters differ from asynchronous counters?
18. Differentiate Mealy and Moore model.
19. Write HDL behavioral model of D flip-flop.
20. State the rules of state assignment.
21. What are the different techniques used in state assignment?
22. What are significance of state assignment.
23. State the different types of shift registers.
24. Write any two applications of shift register.
25. What is synchronous counter?

**13 MARKS**

1. Explain the operation of master slave JK flip flop.
2. Design and implement SR flip flop using NOR gates.
3. Implement T flip flop and JK flip flop using D flip flop.
4. Design a mod-5 synchronous counter using JK flip flop. Construct its timing diagram.
5. Design a divide by 7 counter using JK flip flops
6. Usng JK flip flops design synchronous counter which counts in the sequence 000,001,010,011,100,101,110,111,000….
7. Design a binary counter using T-flip flops to count in the following sequence 000,100,111,010,011,000
8. Design a synchronous counter with the following sequence: 0,1,3,7,6,4 and repeats.
9. Design a 3-bit binary counter using T-flip flop.
10. Design a decade counter using JK flip flops.
11. Design and explain the working of up down counter.
12. What are registers? Construct a 4-bit register using D flip flops and explain the operations of the registers.
13. A sequential circuit has two JK flip flops A and B. The flip flop input functions are

JA=B JB=x’

KA=Bx’ KB=AExclusive Or XOR Gate Logic Gate Clip Art, PNG, 600x600px, Exclusive Or,  Area, Bitwise Operation, Black x

(i)Draw the logic diagram of the circuit

(ii)Tabulate the state table

(iii)Draw the state diagram.

1. A Sequential circuit with two D flip flops A and B, two inputs x and y , and one output Z is specified by the following input equations.

A(t+1)=x’y +xA

B(t+1)=x’B+xA

Z=B

Draw the logic diagram of the circuit. Derive the state table and state diagram and state whether it is a Mealy or a Moore machine.

6.Write a VHDL code to realize a 3-bit Gray code counter using case statement.

**UNIT-4**

**2 MARKS**

1. When asynchronous sequential circuits are preferred in circuits design.
2. Define Merger graph.
3. Define Race condition in Asynchronous sequential circuits.
4. What is critical and non-critical race?
5. What is lockout? How it is avoided?
6. Difference between fundamental mode circuits and pulse-mode circuits.
7. What is Primitive Flow table?
8. What are cycles and races?
9. Why is the pulse mode operation of asynchronous sequential circuits not very popular?
10. Differentiate Static & Dynamic Hazard .Define Essential Hazard.

**13 MARKS**

1. Design an asynchronous sequential circuit with 2 inputs X and Y and output Z. Whenever input Y is 1 , input X is transferred to Z. When Y is 0 ,output does not change for any change in X. Use SR latch for implementation of the circuit.
2. An asynchronous sequential circuit is escribed the following Excitation and output functions:

Y=x1x2’ + (x1+x2’)y

Z=y

(i)Draw the logic diagram of the circuit

(ii)Derive the transition table and output map.

1. Design an asynchronous sequential circuit with inputs x1 and x2 and one output z. Initially and at any time if both the inputs are 0, output is equal to 0. When x1 or x2 becomes 1, z becomes 1. When second input also becomes 1, z=0; the output stays at 0 until circuit goes back to initial state.
2. Outline the procedure for analyzing asynchronous sequential circuits.
3. Summarize the design procedure for asynchronous sequential circuits.

**UNIT-5**

1. **MARKS**
2. State the types of ROM.
3. Draw 4x2 ROM with AND-OR gates.
4. How many address lines and data lines there in 4K X 8 ROM?
5. How many 32 K x 8 RAM chips are needed to provide a memory capacity of 512 Kbytes
6. Differentiate SRAM and DRAM.
7. What is memory decoding?
8. What are error detecting codes? Give examples.
9. How many check bits are required for single bit error detection and correction?
10. How to detect double error and correct single error?
11. List the advantages of sequential programmable devices.
12. List the major differences between PLA and PAL.
13. What is static hazard and dynamic hazard?
14. Draw the wave forms showing static 1 hazard.

2.

What is FPGA?

**13 MARKS**

1. Describe briefly about RAM and its types.
2. Explain the logical construction of 256x8 RAM using 64x8 RAM chips.
3. Give the internal block diagram of 4 x 4 RAM.
4. Write short notes on address multiplexing.
5. Encode the binary word 1011 into seven bit even parity Hamming code.
6. Implement the following functions using PLA

F1=∑m(1,2,4,6) F2=∑m(0,1,6,7) F3=∑m(2,6)

1. Design a PLA structure using AND and OR logic for the following functions.

F1=∑m(0,1,2,3,4,7,8,11,12,15)

F2=∑m(2,3,6,7,8,9,12,13)

F3=∑m(1,3,7,8,11,12,15)

F4=∑m(0,1,4,8,11,12,15)

1. Implement the following two Boolean functions with a PLA:

F1(A,B,C)=AB’+AC+A’BC’

F2(A,B,C)=(AC+BC)’

1. Draw a neat sketch showing implementation of Z1=ab’d’e+a’b’c’e+bc+de, Z2= a’c’e, Z3=bc+de+c’d’e+bd and Z4=a’c’e+ce using 5\*8\*4 PLA.
2. Implement the combinational circuit having the shown truth table, using PLA

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | C | F1 | F2 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 |

1. For the Boolean function, obtain the hazard-free circuit

F(A,B,C,D)=∑m(1,3,6,7,13,15)

1. What are hazards and its types? How to design a hazard free circuit ? Explain with an example.